Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **ADJ**
2. **NC**
3. **NC**
4. **NC**
5. **NC**
6. **+**
7. **NC**
8. **–**
9. **NC**

**2**

**3**

**4**

**1 9**

**5**

**6**

**8**

**7**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004 x .004”**

**Backside Potential: FLOAT or -**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .047” X .045” DATE: 8/17/21**

**MFG: SILICON SUPPLIES THICKNESS .015” P/N: LM136-2.5**

**DG 10.1.2**

#### Rev B, 7/1